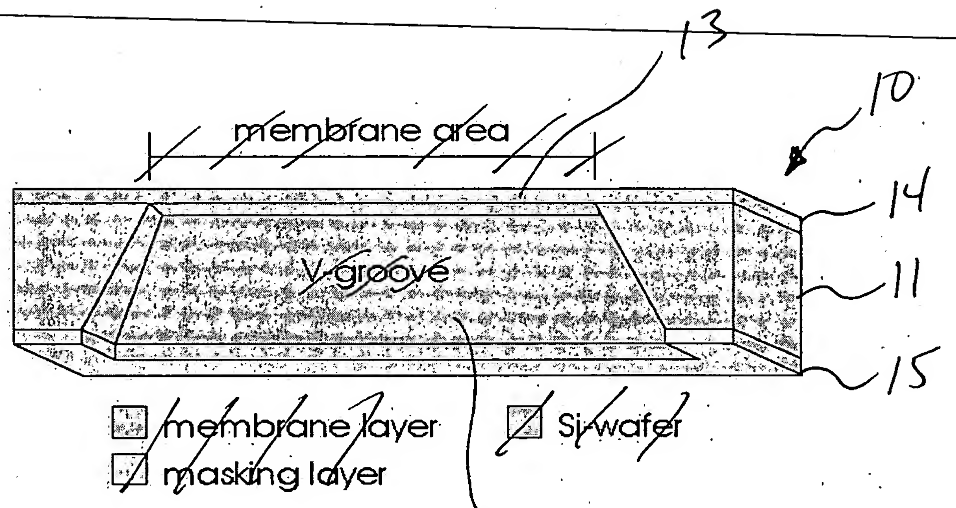


FIG. 1
PRIOR ART

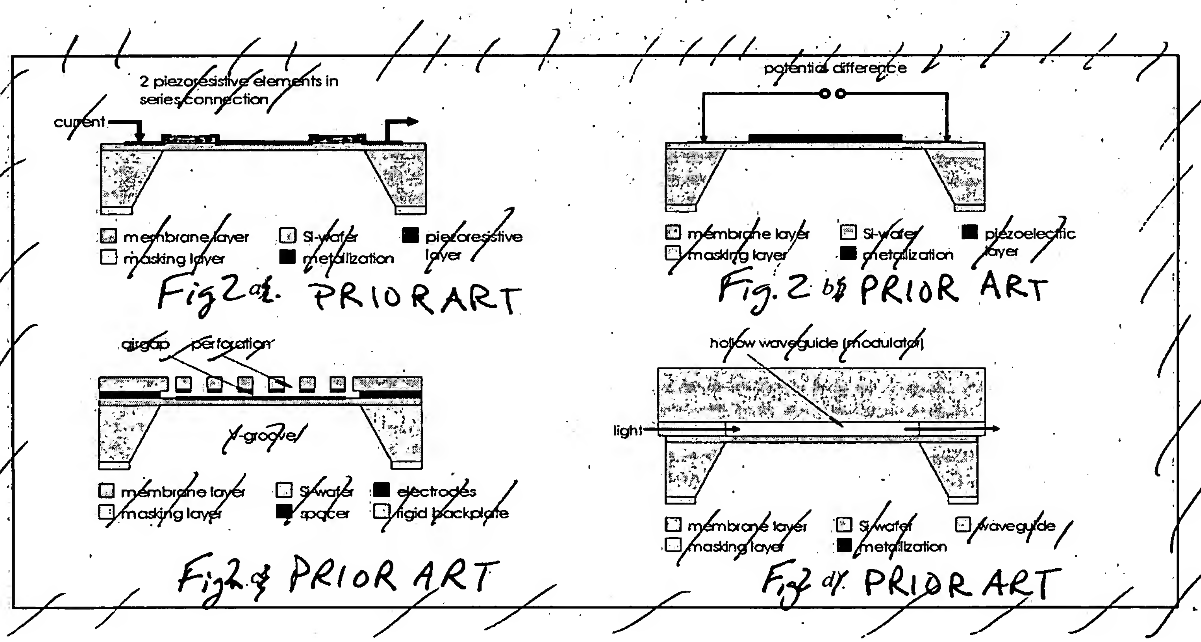
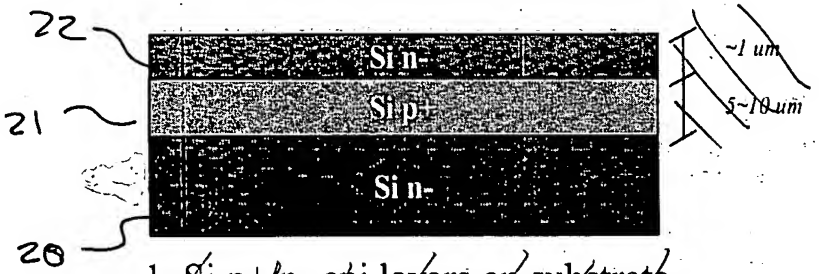
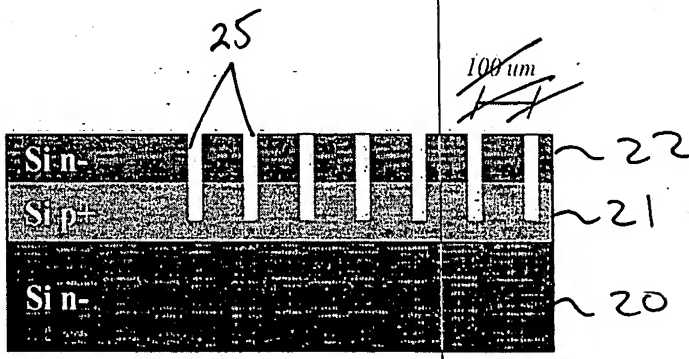


FIG. 2



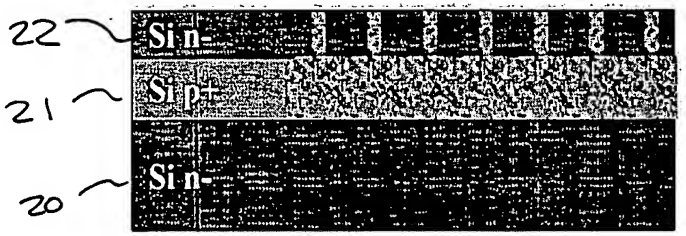
1. Si p+/n- epi layers on substrate

FIG. 3A-a



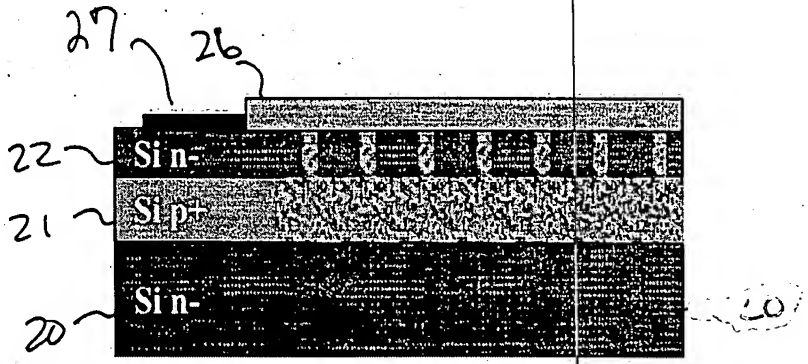
2. Trench formation by plasma etching (and mask opening)

FIG. 3B b



3. Si Porous formation in p+ by electrochemical attack
4. Trench filling and surface planarization

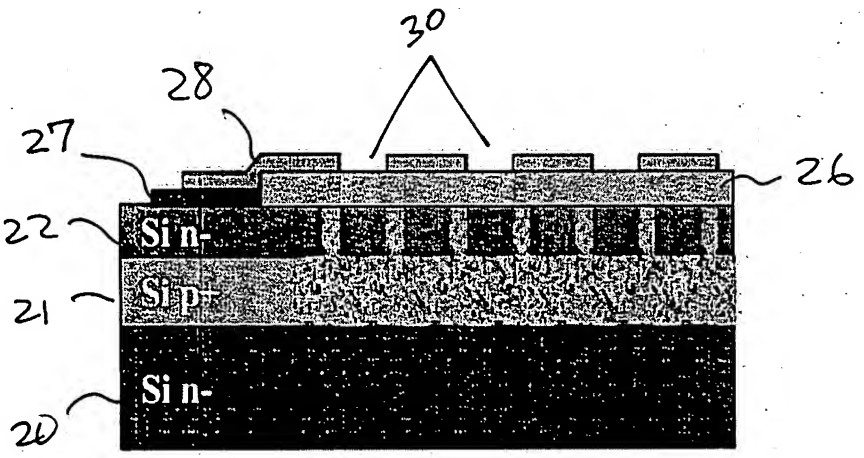
FIG. 3C c



5. Deposition and patterning of the sacrificial layer
6. Nitride isolation layer

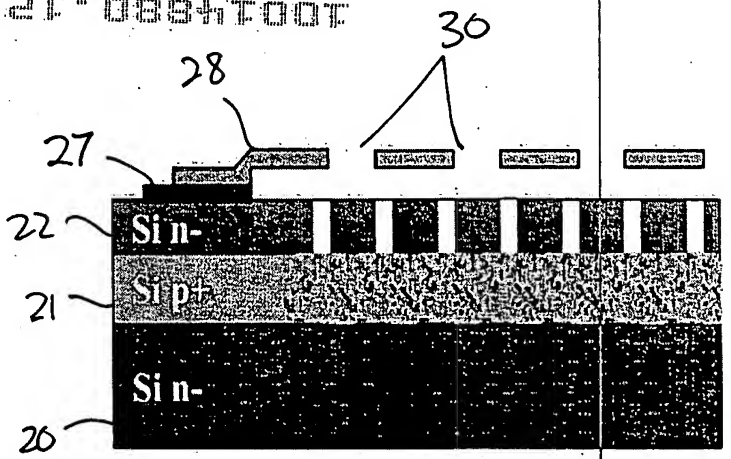
FIG. 3D d

2/4



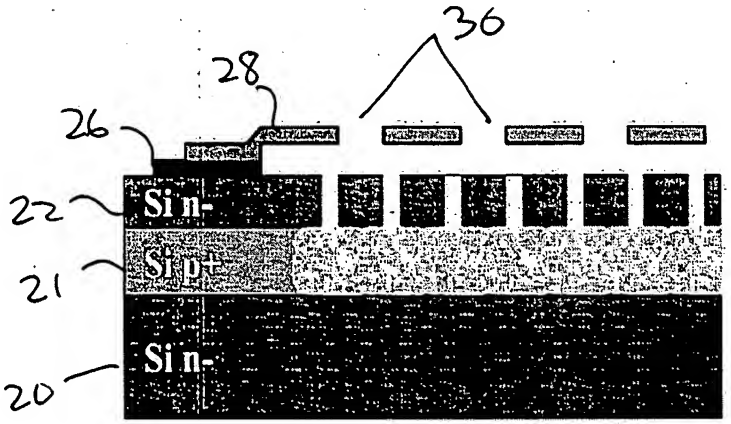
7. PoliSi n+ formation for backplate

FIG. 3E e



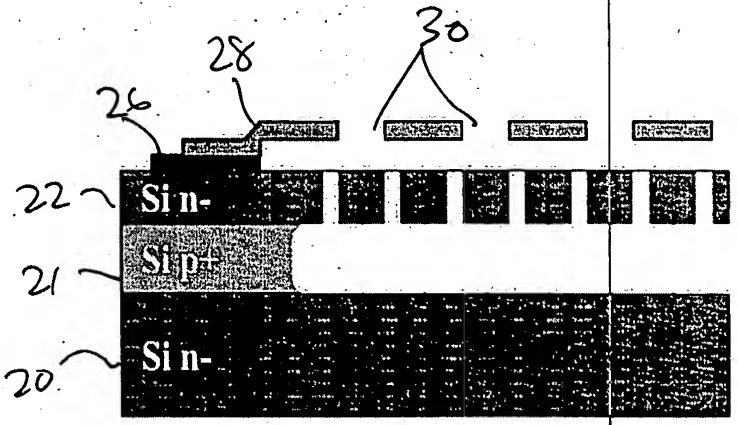
8. Removal of the sacrificial layer (HF attack)

FIG. 3F f



9. Si-porous Oxidation

FIG. 3G g



10. Removal of Si-porous

FIG. 3H h

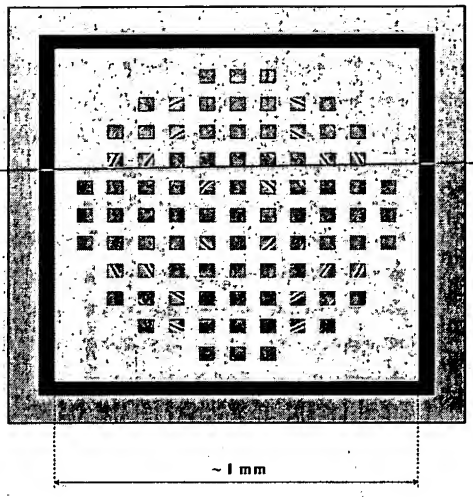


FIG. 4

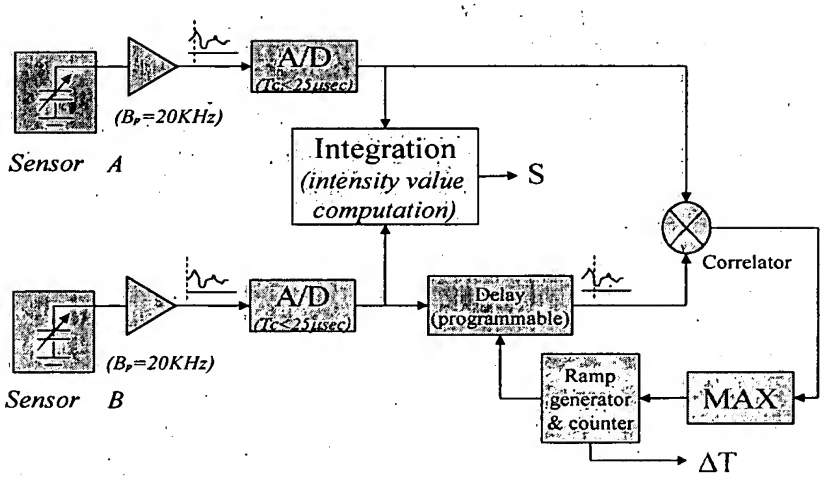
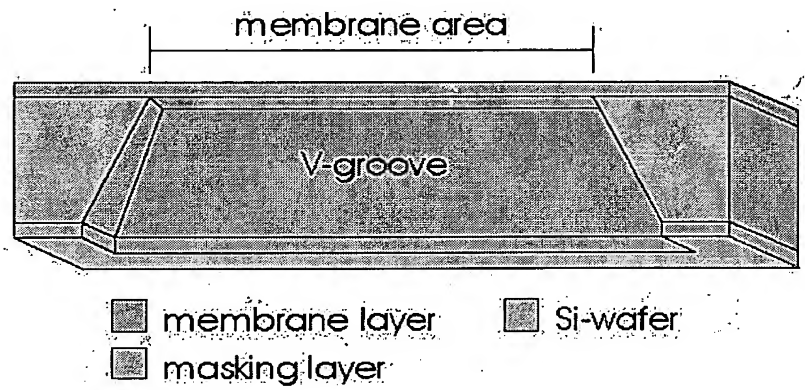
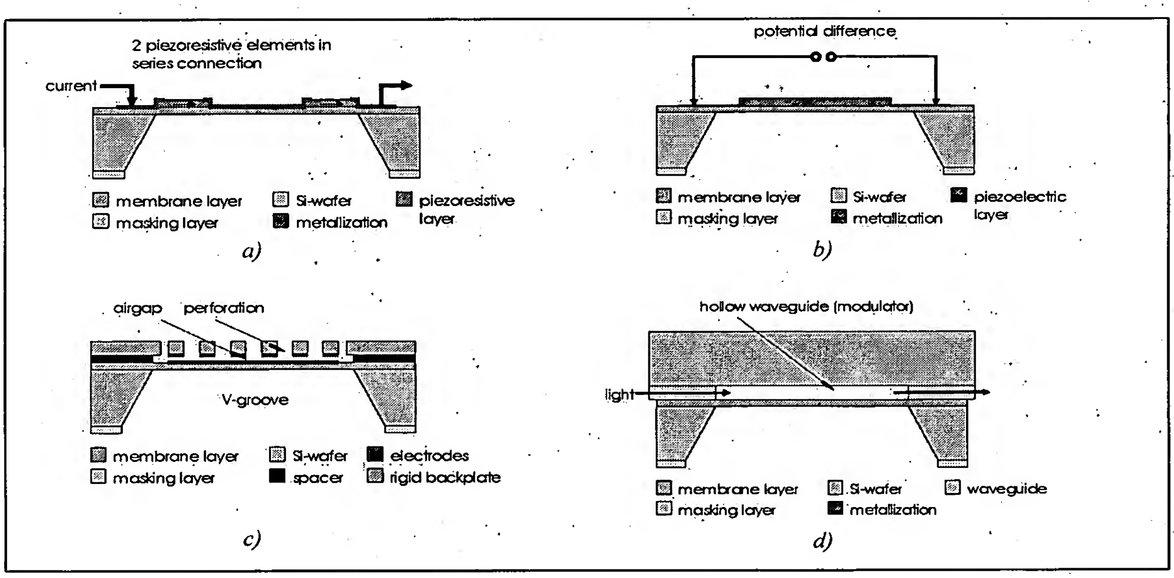


FIG. 5



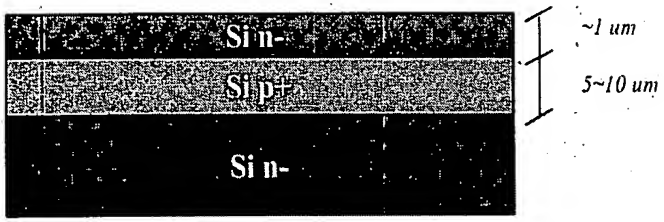
membrane area
V-groove
membrane layer
Si-wafer
masking layer

FIG. 1



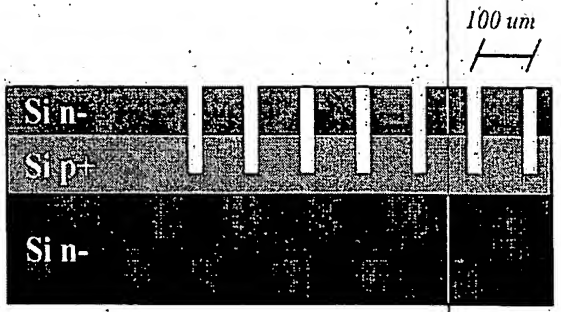
2 piezoresistive elements in series connection
current
membrane layer
masking layer
Si-wafer
metallization
piezoresistive layer
a)
potential difference
membrane layer
masking layer
Si-wafer
metallization
piezoelectric layer
b)
airgap
perforation
V-groove
membrane layer
masking layer
Si-wafer
spacer
electrodes
rigid backplate
c)
hollow waveguide (modulator)
light
membrane layer
masking layer
Si-wafer
metallization
waveguide
d)

FIG. 2



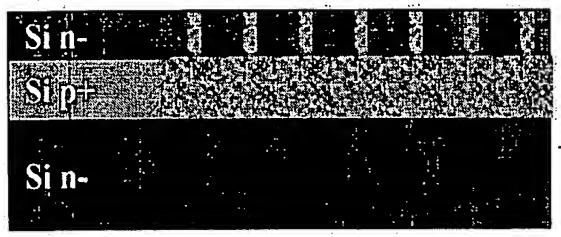
1. Si p+/n- epi layers on substrate

FIG. 3A



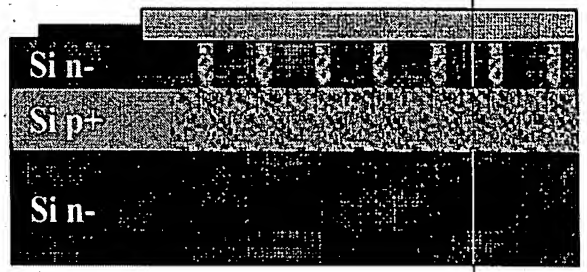
2. Trench formation by plasma etching (and mask opening)

FIG. 3B



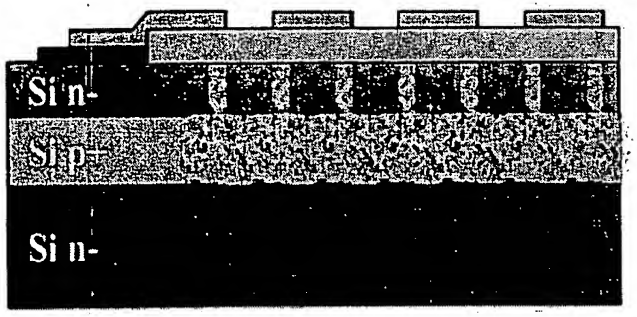
3. Si Porous formation in p+ by electrochemical attack
4. Trench filling and surface planarization

FIG. 3C



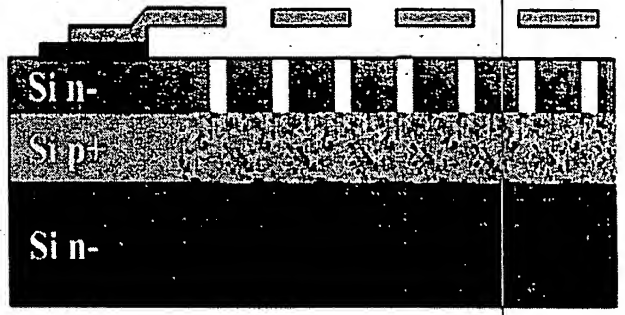
5. Deposition and patterning of the sacrificial layer
6. Nitride isolation layer

FIG. 3D



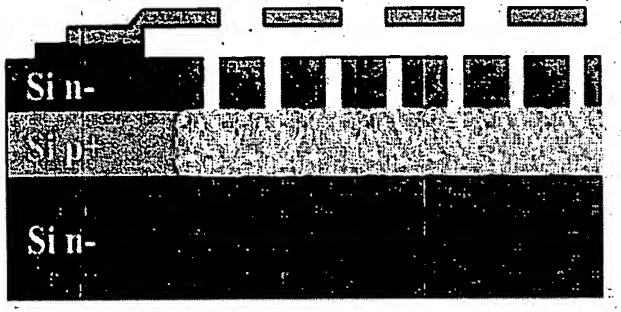
7. PoliSi n+ formation for backplate

FIG. 3E



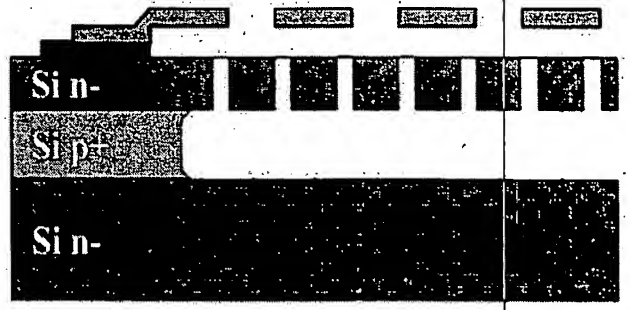
8. Removal of the sacrificial layer (HF attack)

FIG. 3F



9. Si-porous Oxidation

FIG. 3G



10. Removal of Si-porous

FIG. 3H

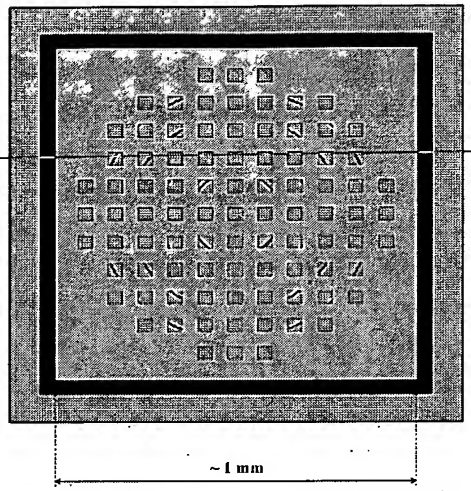

~1 mm

FIG. 4

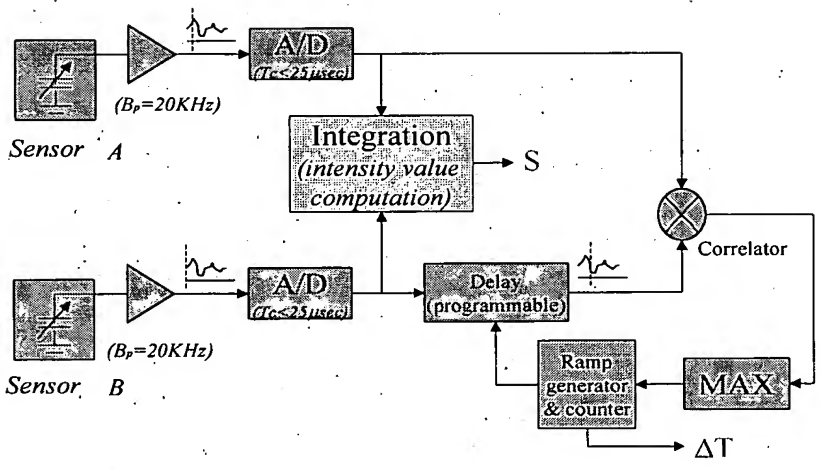

A/D
(Tc<25 μsec)
(Bp=20KHz)
Sensor A
Integration
(intensity value computation)
S
Correlator
A/D
(Tc<25 μsec)
Delay
(programmable)
(Bp=20KHz)
Sensor B
Ramp generator & counter
MAX
ΔT

FIG. 5